Process and Performance Improvements to Type-II GaAsSb/InP DHBTs

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Abstract

GaAsSb/InP type-II transistors have been fabricated with f_T > 325 GHz and f_{MAX} > 275 GHz. This work will examine the layer structure design criteria allowing the f_T to improve from 244 GHz to 358 GHz and the effects this has on the corresponding f_{MAX}. Additionally, the process improvements to control the undercut into the active region during the base contact isolation etch will be discussed. These modifications improved f_{MAX} from 225 GHz to 279 GHz.

1. Introduction

The increased demand for higher bandwidth communication systems and higher capacity network systems have pushed the need for faster transistors. The InP material system has risen to meet those demands with the InP/InGaAs SHBT recently reporting f_T > 500 GHz [1] and its DHBT counterpart also reporting new record speeds, with f_T > 390 GHz [2]. However, the InP/InGaAs transistors have significant limitations. The SHBT has a low BV_{CEO} due to its small bandgap InGaAs collector. This makes the transistor too fragile to be used in many circuit applications. The type-I DHBT requires the insertion of a grading layer in the collector to mitigate the effects of current blocking [3]. This reduces its breakdown voltage, increases the crystal growth and processing complexity, and increases its thermal resistance. While there have been reports of a type-I InP/InGaAs DHBT without any compositional grading at the base-collector junction that achieves f_T near 200 GHz [4], it still cannot achieve high current densities without observing current blocking. Since this transistor cannot push high current densities, its speed lags behind the DHBT with grading.

The type-II InP/GaAsSb DHBT has been proposed to address the problems that plague the other two material systems. The InP/GaAsSb makes use of a wide bandgap InP collector, giving it a significantly larger breakdown voltage than the InP/InGaAs SHBT. The staggered, type-II band lineup potentially allows the InP/GaAsSb DHBT to avoid current blocking due to the conduction band discontinuity that limits the InP/InGaAs DHBT. A diagram of the conduction bands of a type-II DHBT, an abrupt, type-I DHBT, and an SHBT are shown in Fig. 1. The band diagrams were calculated by [5].

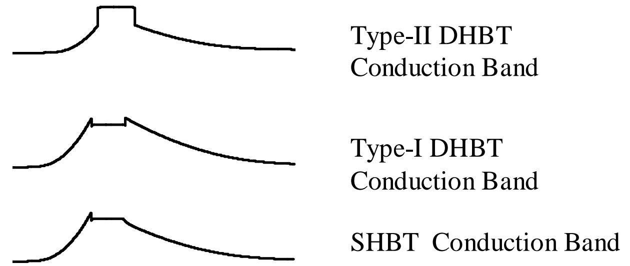


Fig. 1: Equilibrium band diagram of the conduction bands of a type-II DHBT, an abrupt, type-I DHBT, and an SHBT

Even though InP/GaAsSb technology had been present since 1995 [6,7], major improvements in speed have only occurred fairly recently. Simon Frasier University demonstrated the ability of this material system to compete with its InGaAs complement, reporting f_T > 300 GHz and a Johnson Limit > 1800 GHz-V [8]. Recently, further progress in vertical scaling has allowed the InP/GaAsSb material system to achieve an f_T > 350 GHz [9].

Due to the novelty of the InP/GaAsSb material system, its process and its layer structure have not been fully explored. In this work, we will present a number of process and layer structure improvements for achieving for high speed, type-II transistors. Experiments designed to optimize the collector thickness, base doing, and base composition in HBT layer structure have been conducted. Additionally, modifications to the wet-chemical etching process have been explored to achieve optimal device performance.

2. Layer Structure and Device Fabrication

The baseline process is a standard mesa process outlined in [10]. The emitter and base contacts are defined by electron beam lithography. The collector contact is defined by optical lithography. The mesas were etched using a selective wet etch process. The base contact is connected to the intrinsic emitter via a μ-bridge. This bridge serves to isolate the base contact, eliminating the extrinsic base-collector capacitance associated with that contact. However, the advantages obtained by isolating the base contact are gained at the expense of greatly increasing the processing complexity.

In this study, three different epitaxial structures were examined with a focus on the base and collector layers. All structures were grown by MOCVD on semi-insulating, Fe doped InP substrates. Structure A consisted of a 30 nm, lattice matched $GaAs_{0.51}Sb_{0.49}$ base, carbon doped to 4e19 cm^{-3} and a 150 nm InP collector, silicon doped to 3e16 cm^{-3}. Structure B consisted of a 25 nm $GaAs_{0.65}Sb_{0.35}$ base, carbon doped to 6e19 cm^{-3} and a 150 nm, unintentionally doped InP collector. Structure C consisted of a 25 nm $GaAs_{0.65}Sb_{0.35}$ base, carbon doped to 6e19cm^{-3} and a 75 nm, unintentionally doped InP collector. Strain was added to the base of structures B and C in an attempt to reduce the conduction band discontinuity between the emitter and base layers. The structures, along with their corresponding DC gain and RF performance, are summarized in Table 1 for a 0.35x8 μm^2 emitter.

Material	Structure A	Structure B	Structure C
$GaAs_xSb_{1-x}$ (base)	30nm, C=4e19	25nm, C=6e19	25nm, C=6e19
InP (collector)	150nm, Si=3e16	150nm, Si=1e16	75nm, Si=1e16
f_T (GHz)	244	248	359
f_{MAX} (GHz)	225	234	181
β	29	21	21

Table 1: Summary of the layer structure for each wafer.

3. *Results and Discussion*

3.1 *Base Design*

The base layer was first investigated to determine the effects doping and thickness had on the current gain and the RF performance. A direct comparison of structures A and B indicates a reduction of base thickness from 30 nm for structure A, to 25 nm for structure B, only yields a 4 GHz increase in f_T. This difference is not large enough to be distinguished from processing or measurement error. Thus, the reduction in thickness of the base is offset by the increased scattering due to the higher doping or complications arising from the lattice mismatch.

The largest difference between the performances of the two structures is the reduction of the current gain. The increased doping contributes to an increased electron-hole and auger recombination, reducing the maximum current gain from 29 to 21. It should be noted that increased base doping is necessary to decrease base resistance, thereby increasing f_{MAX}.

3.2 *Collector Design*

The collector structures were investigated to explore the optimum tradeoff between the transit times and capacitances. As the collector is vertically scaled, the collector transit time decreases, but the capacitance between the base and the collector, C_{BC} increases. These effects are shown in the equations 1 and 2 as follows:

$$\frac{1}{2\pi\ f_T} = \tau_B + \tau_C + \frac{kT}{I_C} C_{je} + (R_C + R_E + \frac{kT}{I_C}) C_{BC} \qquad (1)$$

$$f_{\mathrm{MAX}} = \sqrt{\frac{f_t}{8\pi\ R_B C_{BC}}} \qquad (2)$$

τ_B and τ_C are the base and collector transit times, I_C is the collector current, C_{je} is the emitter-base junction depletion capacitance, C_{BC} is the base-collector capacitance, and R_C and R_E are the emitter and collector resistances.

An additional benefit to scaling the collector is to delay the point at which the electric field at the base-collector junction fully collapses, which is the well-known Kirk Effect. This allows a higher current to be pushed through the transistor, mitigating the effects of the increase in C_{BC}.

A direct comparison between structures B and C shows the effects of lateral scaling. Structures B and C have the same layer structure with the exception of the collector thickness. The thinner collector allows a reduction in the transit time, shown by the increase in f_T from 248 GHz associated with structure B to 358 GHz for structure C.

Thinning the collector reduces the distance between the heavily doped base and the heavily doped subcollector, increasing C_{BC}. A first order approximation of the effects that collector thickness has on C_{BC} is that a 50% reduction in collector thickness corresponds to a 100% increase in C_{BC}. The effects of this increase are most clearly shown in the f_{MAX} results. While an increase in f_T benefits f_{MAX}, the increase in C_{BC} more than offsets that increase. Equation (2) predicts the f_{MAX} of structure C should be 85% of the f_{MAX} of structure B. The increase in C_{BC} indeed decreases f_{MAX}; the decline is from 234 GHz with structure B to 181 GHz with structure C, corresponding to a 77% decrease. The discrepancy is most likely a result of process variation, as it is more difficult to control undercuts with thicker structures, and the approximations made in calculating the differences in C_{BC}.

3.3 *Process Optimization*

Isolating the base contact from the intrinsic transistor is essential to achieving optimal high-speed performance. Isolation of the base contact reduces C_{BC}, increasing both f_T and f_{MAX}. This process is accomplished by evaporating a metallic µ-bridge connecting the intrinsic device to the base contact. The semiconductor material underneath is then undercut leaving only the bridge, as shown in Fig. 2.

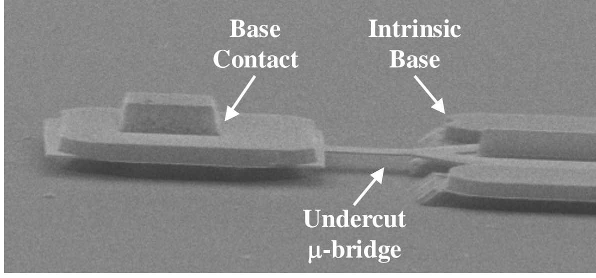


Fig. 2: An undercut μ-bridge

Undercutting the μ-bridge increases the complexity of the processing. While the wet chemicals laterally etch underneath the air bridge, they simultaneously etch into the intrinsic device, indicated in Fig. 3a. This lateral etching reduces the active device area, harming device performance.

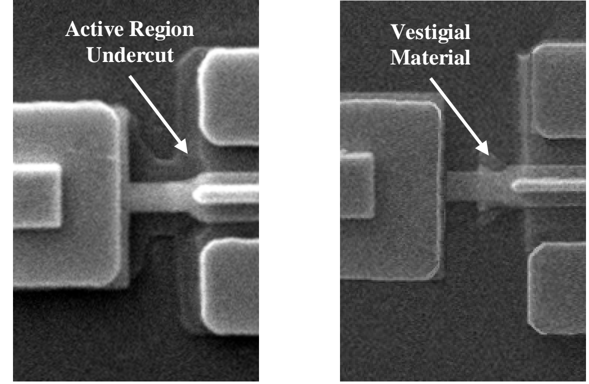
Table 2 correlates the improvement in f_{MAX} to the amount of undercut for a 0.35 x 4 μm^2 device using layer structure C. The initial process yielded a device with an f_T of 308 and an f_{MAX} of 225 GHz. The process improvements yielded final results of f_T = 331 and f_{MAX} = 279 GHz.

Process #	f_{MAX} (GHz)	Active region undercut (μm)
1	225	1
2	247	1
3	268	0.5
4	279	0

Table 2: f_{MAX} vs. Active region undercut

An additional complication to the μ-bridge process is the different etching rates between GaAsSb and InGaAs. The GaAsSb layer surrounding the μ-bridge needs to be etched to expose the InP layer to allow undercutting. While the GaAsSb layer surrounding the μ-bridge is being etched, the InGaAs collector contact layer is simultaneously etched. The GaAsSb layer etches at a much slower rate than the InGaAs layer, making it difficult to control the undercut into the InGaAs layer. This is complicated by there being no wet acid has been found with selectivity between GaAsSb and InGaAs.

Two techniques have been proposed to circumvent the lateral etching. The first is to shift the photo-resist that covers the collector up further onto the bridge. This allows a larger distance for the acid to undercut before it reaches the active region. However, this presents the problem of leaving behind vestigial base material, as indicated in Fig. 3b. This material causes an increase in C_{BC}. While shifting over the resist reduces the lateral undercut into the active region, it creates the problem of leaving vestigial material.



(a) (b)

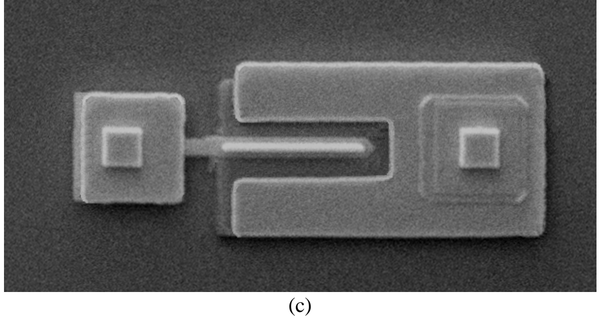

(c)

Fig. 3: SEM photographs of (a) a top-down view of the μ-bridge and the active region with significant active region undercut, (b) a top-down view of the μ-bridge and the active region with vestigial material on its air bridge, and (c) a transistor with little undercut or vestigial material

Another technique was to oxidize the exposed base using an oxygen plasma. This allowed the GaAsSb oxide to be etched using a basic solution, one that the InGaAs collector layer was resistant to. Using this technique, the photo-resist did not have to be shifted as far. However, the oxygen plasma only oxidizes exposed material, so this method allows the InP collector to be exposed, but does not clear the GaAsSb layer underneath the bridge. Nonetheless, this solution allows the resist to be shifted close enough to the intrinsic device to drastically reduce the amount of vestigial base material.

These two enhancements, shifting the resist block and oxidizing the base layer to change the etch chemistry allows a much more controlled μ-bridge clear recipe. The final result is shown as Fig. 3c. There is very little undercut into the active region and, while there still is some material, there is significantly less vestigial material on the intrinsic device. The improvement of f_{MAX} from 225 GHz to 279 GHz is largely attributed to these modifications.

4. Conclusion

Transistors have been fabricated from three different epitaxial structures with varying base doping and collector

thickness. Vertical scaling of the collector allowed the f_T to improve from 244 GHz to 358 GHz. Additionally, improving the μ-bridge clearing recipe allows f_{MAX} to increase from 225 GHz to 279 GHz. To the authors' knowledge, these results are among the fastest reported speeds for type-II DHBTs to date.

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ACRONYMS

f_T: Cutoff frequency
BV_{CEO}: Breakdown Voltage, Collector-Emitter, With Base Open
HBT: Heterojunction Bipolar Transistor
MOCVD: Metal Organic Chemical Vapor Deposition
SHBT: Single Heterojunction Bipolar Transistor
DHBT: Double Heterojunction Bipolar Transistor
SI: Semi-Insulating