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Process Optimization for RF Performance of Ion-Implanted E/D MESFETs

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Abstract

Results are presented from a design of experiments targeted towards extending the use of ion-implanted MESFETs to higher frequencies. The implant schedule is optimized to achieve a shallow, abrupt profile while maintaining high peak carrier concentration. Minimizing the source-drain spacing improves the high frequency performance. The resulting d-mode and e-mode devices both have f_t over 120 GHz and f_{max} over 160 GHz, making the device an excellent candidate for low-cost, high-performance wireless and fiber channel applications.

INTRODUCTION

As the demand for wireless technology continues to increase, GaAs MESFETs are being used in an ever expanding number of applications. High-speed digital communications networks are using MESFETs at 10 GHz [1], and companies are scaling up their production capabilities to 150 mm wafers to supply the quantities required [2]. The attractiveness of the MESFET comes from its low price relative to the performance it provides. The structure is simple, easy to manufacture, and a stable, mature process already exists for volume production.

As applications have moved to higher frequencies the MESFET has been refined to keep pace. Ion-implanted MESFETs have been demonstrated with excellent low-noise performance [3], as well as good high-speed characteristics. Devices have obtained f_t as high as 168 GHz [4], mainly through minimizing the length of the gate electrode. At the University of Illinois, we have successfully produced both enhancement mode and depletion mode MESFETs with f_t over 100 GHz using a 0.12-μm gate process[5].

This paper will discuss efforts to optimize the RF performance of our ion implanted MESFETs. Experimental designs are presented for modifying the implant schedule and device geometry to achieve the best possible high-speed performance. The result of the experiments is a d-mode device with f_t of 136 GHz and f_{max} of 200 GHz, along with an e-mode device with f_t of 120 GHz and f_{max} of 166 GHz.

IMPLANT OPTIMIZATION

The creation of the active device region is of critical importance in fabricating a device. Beginning with semi-insulating three-inch GaAs substrates, silicon and beryllium are implanted as n- and p-type dopants to generate carriers. There are three separate components of the implant schedule: a low-energy, high-dose n-type surface implant to facilitate ohmic contacts, a medium-energy, medium-dose n-type channel implant to define the channel region, and a medium-energy, low-dose p-type implant to compensate the extended tail of the channel implant. Activation of the implanted impurity atoms is achieved through a capless anneal in an arsenic overpressure at 850 C for 20 minutes.

Two important features of the profile are a high peak carrier concentration to achieve high current levels, and an abrupt cutoff to suppress short channel effects and maximize transconductance [6]. The depth of the implant should also be scaled down as the gate length is decreased. To meet the abrupt and shallow requirements the implant energy must be relatively low, and the high concentration makes a high dose necessary.

Doping levels in the crystal cannot be made arbitrarily large due to saturation and compensation effects that occur [7]. The highest electron concentrations we have been able to achieve with our particular implant and anneal technology is 1.2×10^{18} cm^{-3}, and any additional dopant atoms will occupy the wrong lattice sites in the crystal or exist as interstitials. This is not much of a concern at the surface, where ohmic contacts are the only issue, but in the channel region these additional scattering centers may impair the high-speed performance of the device. The focus of this experiment is therefore the channel and tail portions of the implanted profile.

For this experiment the surface implant is fixed at 20 keV and 2×10^{13} cm^{-2}. The channel implant is varied from 20

to 60 keV with doses from zero to 8.5×10^{12} cm^{-2}, and the p-implant is varied from 20 to 40 keV with doses from 1.0 to 2.0×10^{12} cm^{-2}. The process simulation software package GATES [8] is an invaluable aid in designing the implant schedules.

Fig. 1 shows three of the resulting implant profiles as measured by electrochemical C-V measurement. A channel implant of 40 keV and 7.5×10^{12} cm^{-2} with a p-implant of 30 keV and 1.5×10^{12} cm^{-2} provides a shallow implant with a sharp roll-off, and still maintains a high peak carrier concentration. Channel implants with lower energies and doses create shallower profiles, but the peak carrier concentration begins to suffer. Conversely, higher energies and doses do not increase the carrier concentration appreciably and only make the profile deeper. The selected profile is used for both d-mode and e-mode devices.

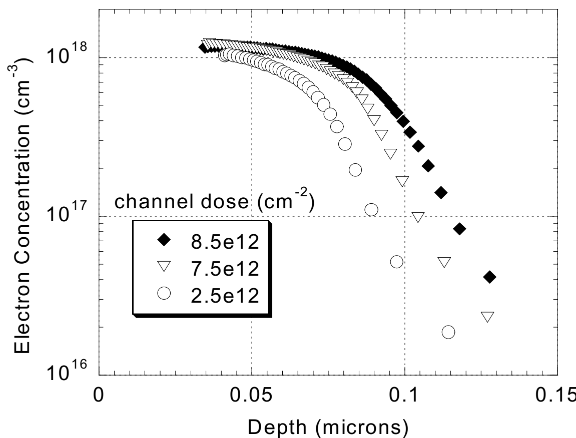
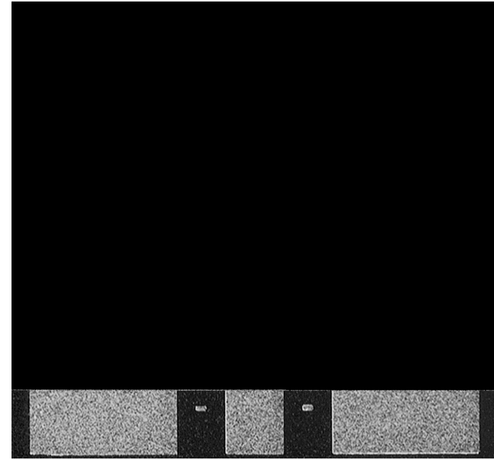


Fig. 1 Implanted electron concentration as a function of depth



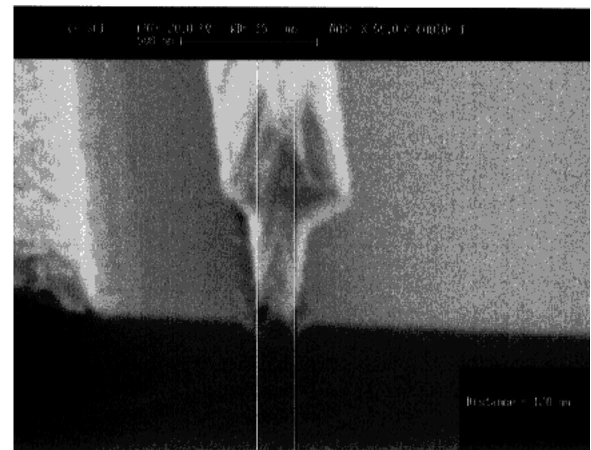


Fig. 2 Photograph of a standard device and SEM micrograph of a 0.12 μm gate

PROCESS

Devices are fabricated using the established University of Illinois MESFET process. Beginning with the material selected from the implant experiment, the process is a simple, manufacturable recipe with a mesa etch for isolation, AuGe/Ni/Au ohmic contacts, and 0.12-μm gates defined by electron beam lithography [5]. Fig. 2 shows a standard two-finger device and a cross section of a 0.12 μm gate.

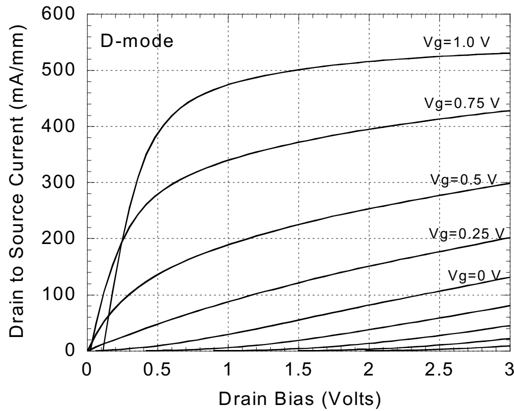
The threshold voltage of the devices is controlled by a recess etch immediately before the Ti/Pt/Au gates are deposited. Process control monitor structures are tested during the recess etch process until current targets are reached. Since the same implant schedule is used for each, the recess etch must be deeper for the d-mode device than the e-mode. Typical d-mode and e-mode I-V curves are shown in Fig. 3.

To optimize for high frequency performance, devices are fabricated with smaller source-drain spacings. This reduces the source resistance and thus increases g_m and f_t.

Fig. 4 shows the f_t and f_{max} dependence on source-drain spacing for d-mode devices, and Fig. 5 shows the data for the 1.5-μm device, which exhibits f_t and f_{max} of 136 and 200 GHz. The best e-mode device has f_t and f_{max} of 120 and 166 GHz. A comparison of the d-mode device to self-aligned ion-implanted MESFETs [9]-[11] and AlGaAs/GaAs HEMTs [12]-[14] of similar gate length is shown in Fig. 6, indicating that the U of I MESFET is a competitive technology and may be a superior solution for many millimeter-wave applications.

CONCLUSIONS

Excellent performance has been achieved through the optimization of the UIUC ion-implanted MESFET process. The key feature is the properly designed implant schedule, which makes the high performance devices possible. Optimizing the geometry of the devices then yields both d-mode and e-mode devices with f_t and f_{max} over 120 and 160 GHz.



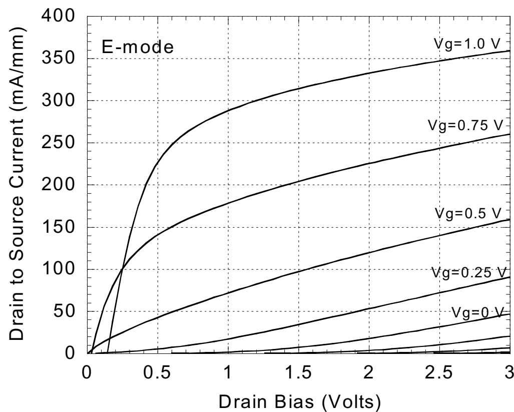


Fig. 3 D-mode and e-mode I-V curves

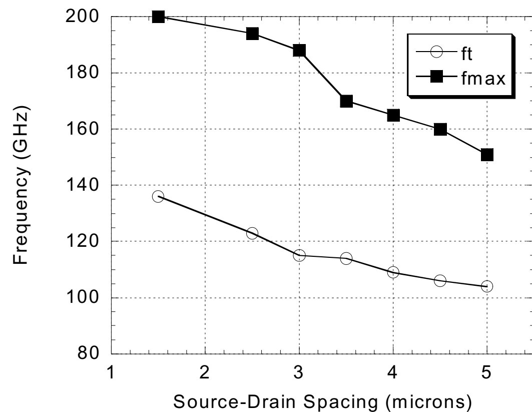


Fig. 4 Effect of source-drain spacing on high frequency performance of d-mode devices

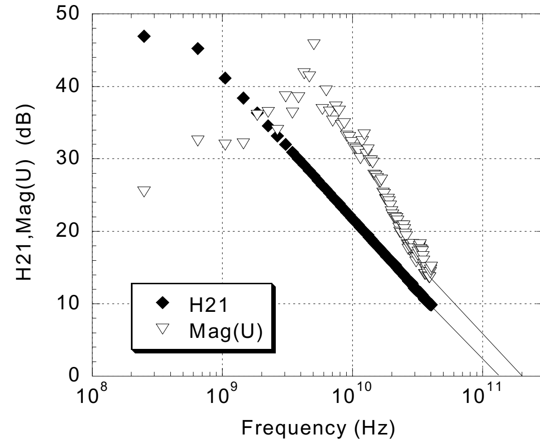


Fig. 5 Data for a d-mode device showing Ft of 136 GHz and Fmax of 200 GHz with V_{ds} = 1.5 V and V_g = 0.6 V.

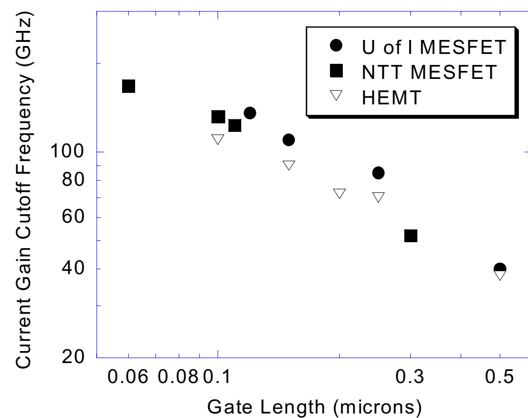


Fig. 6 Comparison of current results to AlGaAs/GaAs HEMTs and NTT MESFETs

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