A 40 Gb/s Integrated Differential PIN+TIA with DC Offset Control Using InP SHBT Technology

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Abstract

This paper describes the design and measured performance of a 40 Gb/s integrated differential PIN+TIA with offset control using InP SHBT technology. The circuit was designed to handle large average optical input power levels (>5 dBm) encountered in short-haul networks where optical gain control may not be available or economical.

INTRODUCTION

Although TIAs with adequate bandwidth for 40 Gb/s applications have been demonstrated in other device technologies, such as InP HEMT or SiGe HBT, when these TIAs are co-packaged with an off-chip photodiode, parasitics due to wire bonding and pad capacitance seriously degrade the performance of the resulting photoreceiver. Also, the limited repeatability of bond-wiring between the TIA input and photodiode, the most speed-critical node in the photoreceiver, can also result in chip-to-chip performance variations that are unacceptable at 40 Gb/s.

The circuit described in this paper integrates the PIN and HBT on a single chip, avoiding these parasitics, with a single supply voltage. Also, the circuit uses a fully-differential preamplifier with output terminals for off-chip automatic dc offset control. Use of an off-chip dc differencing amplifier is advantageous since it minimizes the InP chip area and the speed requirements on this diff amp are low. To the best of the author's knowledge, this is the first reported results on a 40 Gb/s integrated differential PIN+TIA with dc offset control ability using InP SHBT technology.

DESIGN

Figure 1 shows a photograph of the integrated differential PIN+TIA with a GGB Industries dual microwave Picoprobe and dc multi-contact wedges. Also shown in the photograph is a Cascade Microtech lensed-SMF lightwave probe, backed away from the detector. Figure 2 shows the corresponding circuit schematic. The dc op amp, shown in Figure 2, is not integrated on the same chip, but is included to indicate how offset control would be maintained via a low-frequency feedback loop. Identical low-pass RC filter sections (R=12kΩ, C=8pF) are integrated on-chip, to provide the differential dc voltages to the off-chip op amp.

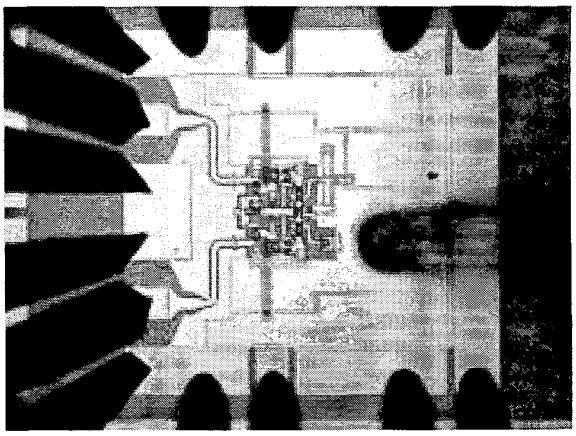

Figure 1. Photograph of the differential PIN+TIA.

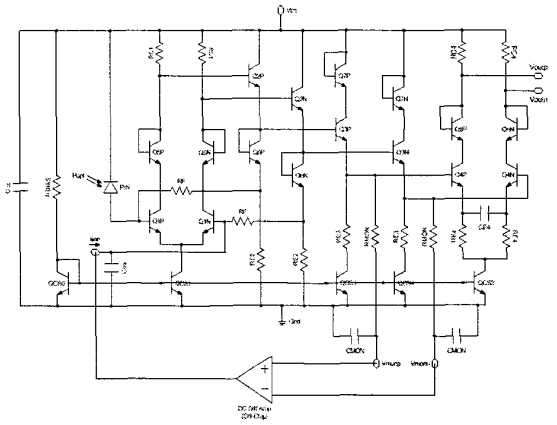

Figure 2. Circuit schematic of the differential PIN+TIA.

The dc and rf performance of the SHBT devices are discussed in detail in [3]. On-wafer, temperature-dependent s-parameter measurements were performed on the SHBTs from 1-50 GHz. For simulation, an in-house SDD-based (Symbolically-Defined Device) large-signal model was extracted via optimization and implemented in Agilent's ADS.

The two differential half-circuits are identical and consist of four stages. The first two stages are a common transimpedance cell consisting of a common-emitter (CE) stage

followed by a common-collector (CC) stage, with feedback resistor connecting to the base of the CE stage. The third stage is another CC stage which provides a dc level shift and, when combined with the preceding CC stage, provides adequate buffering between the first CE stage and the output CE stage. The primary purpose of the final CE stage is to provide a 50-Ω output impedance for the entire circuit. A shunt RC network degenerates the emitters of the output stage, providing a flatter voltage gain versus frequency from this stage.

The positive differential input terminal is connected to the PIN photodetector, which has a 10-μm wide, circular optical window. The negative differential input is shorted to ground at ac, via an on-chip capacitor. At dc, this terminal receives current from the dc feedback loop, required to match the current entering the positive differential input from the PIN detector. Use of this feedback loop also allows the output offset to be increased, if desired, for cases where the 50%-crossing point in the output eye diagram is not the optimal threshold for BER.

The circuit operates with a single -4 to -4.5V supply. When mounted in a chip carrier, larger off-chip capacitors are required at the negative supply terminal, the input negative differential input terminal, and possibly the low-pass RC filtered outputs, depending on the required settling time for the automatic offset feedback loop. For comparison, a single-ended PIN+TIA consisting of one of the differential half-circuits, was fabricated as well.

MEASURED RESULTS

The O/E frequency response of both circuits was measured from 0.5-50 GHz using an Agilent 86030A Lightwave Analyzer. The software accompanying the lightwave analyzer allows measurement of magnitude and phase of responsivity of packaged O/E devices, with an FC/PC optical connector and coaxial electrical connector. For on-wafer characterization, the electrical reference plane must be moved to the tips of the ground-signal-ground rf probe. If the lightwave probe loss is small, and the SMF is assumed to be linear phase, the lightwave probe is not expected to degrade the magnitude response or group delay deviation of the DUT measurement. An automated calibration technique was developed at Xindium, and implemented using Agilent VEE, to obtain corrected O/E magnitude and phase response on-wafer.

For the differential PIN+TIA measurement, the positive output of the differential rf probe was connected through a bias-T to the s-parameter test set, while the negative output of the probe was connected through a bias-T to a coaxial 2.4-mm 50-Ω termination. Thus, the singled-ended responsivity of the differential PIN+TIA is measured. Due to process uniformity and layout symmetry, the diffential responsivity is expected to be twice the single-ended responsivity.

Figures 3 and 4 show the measured responsivity of the differential and single-ended PIN+TIAs, respectively, at both 25 and 85C. Conversion gain can be obtained by multiplying the responsivity by 50Ω. The low-frequency responsivity at T=25C of the differential PIN+TIA is 1A/W (2A/W differential), giving a conversion gain of 50V/W (100V/W differential). The uncorrected (include probe connector and coupling loss) responsivity of separate PINs measured on the same wafer is 0.35A/W at λ=1550nm. The TIA transimpedance can be estimated by dividing the PIN+TIA conversion gain by the PIN responsivity, giving a single-ended transimpedance of 145Ω (290Ω differential). The single-ended PIN+TIA had a low-frequency responsivity of 1.4A/W, and thus a conversion gain of 70V/W, and approximate transimpedance of 200Ω at T=25C.

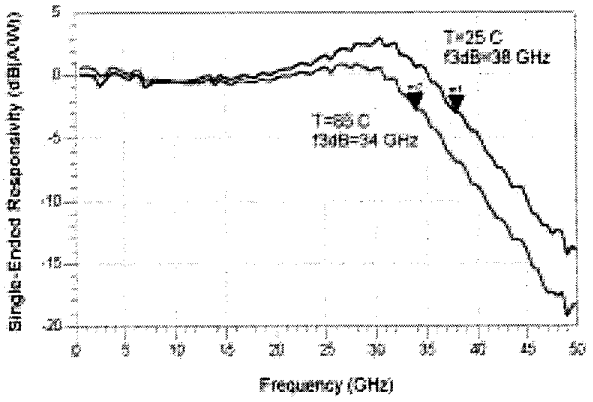

Figure 3. Differential PIN+TIA responsivity (single-ended) at Vcc=-4.5V, Icc=-80mA, Popt=-2dBm, and λ=1550nm

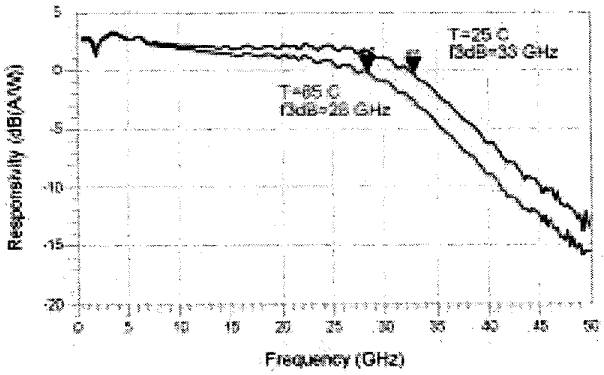

Figure 4. Single-ended PIN+TIA responsivity at Vcc=-3.4V, Icc=-36 mA , Popt=-2dBm, and λ=1550nm

The large peaking of almost 3dB in the differential PIN+TIA frequency response is due to an underestimate of the capacitance density of the MIM capacitors. Thus, the

stage 4 degenerating capacitor in Figure 2 is too large, resulting in higher feedback at higher frequencies. Although gain peaking is often used to extend the bandwidth of wideband amplifiers, it results in large group delay deviation around the peak frequency, which translates to ringing and pattern-dependent jitter in the output eye diagram. Figures 5 and 6 show the measured group delay of the differential and single-ended PIN+TIAs, respectively. As expected, the large peaking between 25-40GHz results in a large group delay deviation for the differential PIN+TIA. The peaking in this amplifier can be decreased by decreasing the value of the stage 4 degenerating capacitor.

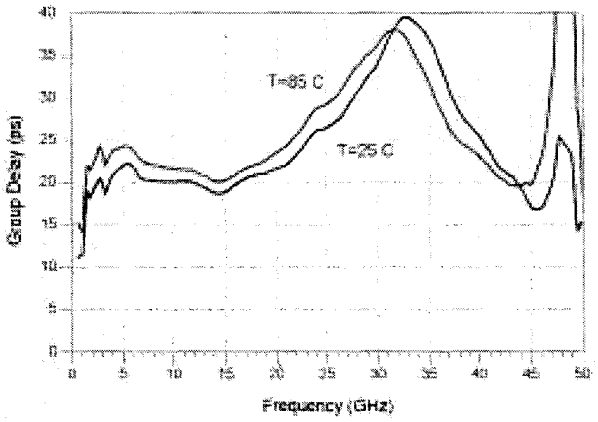

Figure 5. Differential PIN+TIA group delay at Vcc=-4.5V, Icc=-80mA, Popt=-2dBm, and λ=1550nm

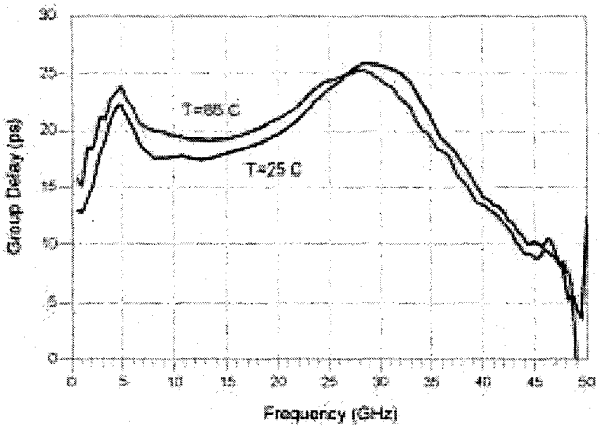

Figure 6. Single-ended PIN+TIA group delay at Vcc=-3.4V, Icc=-36 mA , Popt=-2dBm, and λ=1550nm

Figures 7 and 8 show the measured output electrical return loss of the differential and single-ended PIN+TIAs, respectively.

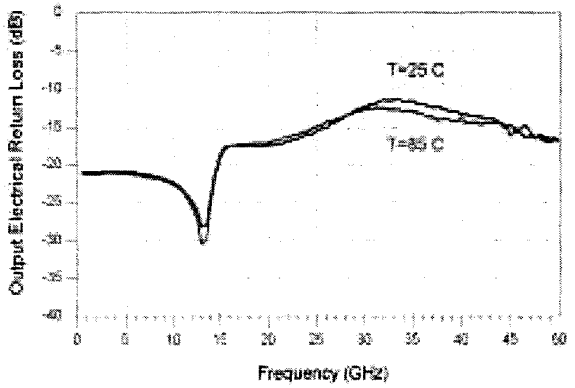

Figure 7. Differential PIN+TIA output return loss at Vcc=-4.5V, Icc=-80mA, Popt=-2dBm, and λ=1550nm

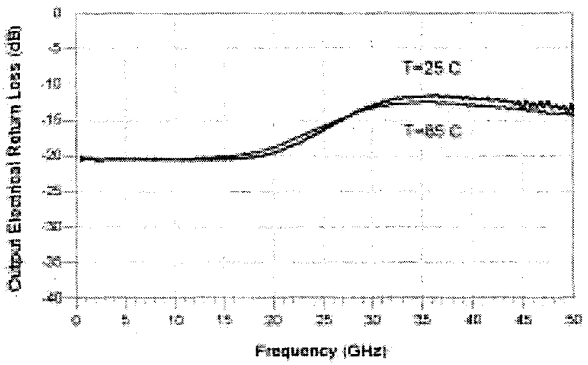

Figure 8. Single-ended PIN+TIA output return loss at Vcc=-3.4V, Icc=-36 mA , Popt=-2dBm, and λ=1550nm

The power consumption of the differential and single-ended PIN+TIAs was (4.5 V)(80 mA) = 360 mW and (3.4 V)(36 mA) = 120 mW, respectively. The chip sizes of the differential and single-ended PIN+TIAs are $1\times1mm^2$ and $0.67\times0.73mm^2$, respectively.

Figures 9 and 10 show the measured dc transfer curves for the differential and single-ended PIN+TIAs, respectively. At the time of test, an EDFA was not available to boost the optical power from -2dBm to a value high enough to supply enough current from the PIN to saturate the TIA. Figures 11 and 12 show the measured dc transfer curves for the differential and single-ended TIAs. This data was obtained from test TIA circuits that were identical to the PIN+TIA circuits, except for an input rf pad replacing the PIN. Also, the circuits were positive supply versions, but this should not affect dc linearity, as compared with a negative dc supply TIA.

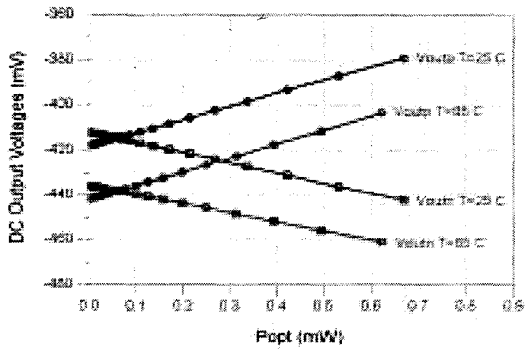

Figure 9. Differential PIN+TIA dc transfer curves at Vcc=-4.5V, Icc=-80mA, and λ=1550nm

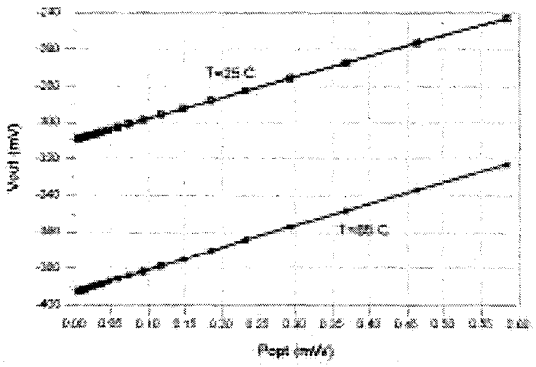

Figure 10. Single-ended PIN+TIA dc transfer curves at Vcc=-3.4V, Icc=-36 mA, and λ=1550nm

It is clear that the differential TIA remains linear for much higher input current levels than the single-ended TIA, a key requirement for short-haul applications where input optical power levels may be very high due to a lack of optical attenuators preceding the receiver chip. Biasing the gain stages with high-output-resistance current sources is a key reason for the higher linearity of the differential TIA. Future designs will add a gain stage between the output buffer and transimpedance stages to boost the conversion gain to levels required by the customer.

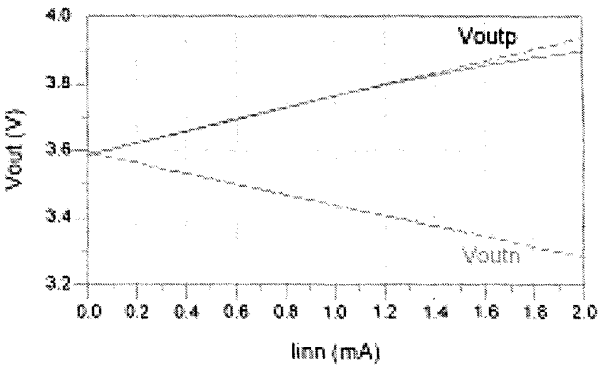

Figure 11. Positive-supply differential TIA dc transfer curves at Vcc=+4V

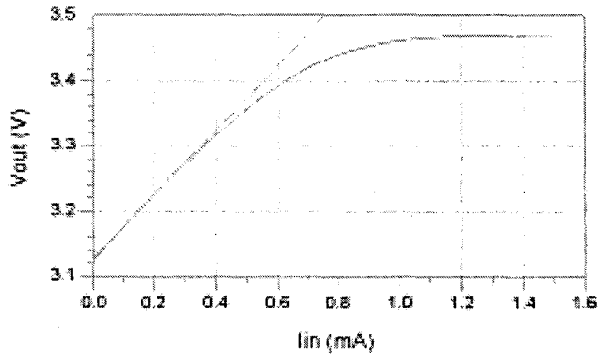

Figure 12. Positive-supply single-ended TIA dc transfer curves at Vcc=+3.5V

REFERENCES

[1] J. Mullrich, et. al., "High-gain transimpedance amplifier in InP-based HBT technology for the receiver in 40-Gb/s optical-fiber TDM links," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp.1260-1265, Sept. 2000.

[2] A. Huber, et. al., "Monolithic, high Transimpedance gain (3.3 kΩ), 40 Gbit/s InP-HBT photoreceiver with differential outputs," *Electronics Lett.*, vol. 35, no. 11, pp. 897-898, May 1999.

[3] S. C. Shen, et. al., "Performance of InP/InGaAs heterojunction bipolar transistors for 40 Gb/s OEIC applications," in 2002 GaAs ManTech.